Remarks

Thorough examination by the Examiner is noted and appreciated.

The Specification has been amended to correct grammatical errors.

The claims have been amended to overcome Examiners objections/and rejections under 35 USC Section 112.

The claims have further been amended and new claims added to clarify Applicants disclosed and claimed invention. The amendments find support in the original claims and/or the Specification.

No new matter has been added.

For example support for limitations in claims 1 and 12 are found in the Specification at:

Paragraph 0014:

"Although the method of the present invention is explained with reference to and is particularly advantageously implemented in forming of copper dual damascenes it will be appreciated that the method of the present invention is equally applicable to the formation of **single copper damascenes** and relatively thick and wide copper damascene structures including, for example, bonding pads or wide trench lines."

Paragraph 0022:

"It has been found that the baking process to remove moisture from low-K porous IMD layers and the DEGAS process can advantageously be accomplished at the simultaneously in the presence of a hydrogen containing atmosphere. For example, **porous** low-K inorganic IMD layers typically strongly absorb moisture prior to and during the etching process, heretofore making a furnace baking process necessary to adequately remove moisture to provide for effective deposition and adhesion of a subsequently deposited barrier layer. According to an aspect of the present invention, it has been found that in the presence of an H2 containing ambient at sub-atmospheric pressures and temperatures of about 100 °C, **moisture as well as adsorbed gases present from a previous etching process, for example oxygen, nitrogen, and fluorine, are effectively removed at the preferred sub-atmospheric DEGAS pressures** and baking temperatures at relatively short times thereby avoiding the necessity of a separate furnace baking process, for example at atmospheric pressures, which may take several hours according to prior art processes."

Support for limitations in claims 3, 4, 14 and 15 are found

in the Specification at paragraph 0021:

"For example the DEGAS/baking process is preferably carried out simultaneously at sub-atmospheric pressures in a **hydrogen containing ambient, preferably a mixture of H_2 gas and an inert gas such as He, N_2, and Ar.** According to an aspect of the invention, preferably, the process water is simultaneously heated to a temperature between about 100 ° C and about 500 ° C, more preferably between about 250 ° C and about 450 ° C in the DEGAS chamber for a period of about 20 seconds to about 120 seconds in the presence of a mixture of H_2/inert gas while maintaining a pressure of between about **1 mTorr and about 10 Torr, more preferably between about 10 mTorr and about 1 Torr, most preferably between about 10 mTorr and about 100 mTorr.**

Support for new claims 21 and 22 are found in the Specification at paragraph 0020:

"In an aspect of the present invention, following formation the dual damascene opening e.g., trench opening 20 and via openings 16A and 16B, the semiconductor process wafer is transferred to a single wafer DEGAS chamber, preferably in-situ, where at least a pressure, ambient gaseous atmosphere and wafer temperature may be controlled. For example a cluster tool having a **controlled sub-atmospheric ambient with reduced oxygen levels, as is known in the art may be used to transfer the wafer from an etching chamber to the DEGAS chamber in-situ to prevent exposure to moisture and oxygen.** For example, the DEGAS chamber preferably includes means for heating the wafer, for example a conventional wafer chuck including resistively heated elements and/or high

intensity lamps directed at the wafer surface for heating the process wafer surface. In addition, the DEGAS chamber may be a conventional physical vapor deposition (PVD) chamber, for example an RF sputtering, magnetron sputtering, ionized metal plasma (TMP), self-ionized plasma (SIP) sputtering chamber for carrying out a subsequent sputter-clean and/or PVD process for depositing a barrier layer to line the dual damascene opening, or be a separate dedicated process chamber in a cluster tool including multiple chambers for the respective DEGAS, sputter-clean and subsequent PVD and/or CVD processes."

Claim Rejections under 35 USC 102(e)

1. Claims 1, 3-12, and 14-20 stand rejected under 35 USC Section 102(e) as being anticipated by Pan et al. (US Pub. 2004/0023485).

Pan et al. disclose a method for hydrogen/inert gas (preferably He) plasma treatment of anisotropically etched openings to improve a crack resistance (see Abstract), prior to depositing the barrier layer. Pan et al. also disclose an **optional pre-heating treatment prior to the hydrogen plasma treatment** (see paragraph 0021, 0032).

Thus Pan et al. do not disclose several aspects of Applicants disclosed and claimed invention including:

Pan et al. do not disclose or suggest "then carrying out a sub-atmospheric DEGAS process in-situ with simultaneous heating of the process wafer in a hydrogen containing ambient;" following etching through a lower etch stop layer to expose a copper area as Applicants have disclosed and claimed.

Thus Pan et al. is insufficient to anticipate Applicants disclosed and claimed invention.

Claim Rejections under 35 USC 103(a)

1. Claims 1-2, 6-13, and 17-20 stand rejected under 35 USC Section 103(a) as being unpatentable over Kim (US 6,767,788) in view of Rozbicki et al. (US 6,554,914).

Kim disclose a process for making a damascene capacitor structure followed by forming a dual damascene at the same level (see abstract; Figures 1E, 1F; col 6, lines 33-65). In

particular Kim discloses a degas process under high vacuum followed by a sputter clean process using a plasma including hydrogen **following deposition** of a **copper seed layer on a barrier layer** (col 6, lines 36-46).

Thus, the method of Kim works by a different principal of operation than the method of Applicants, and could not accomplish the purpose of Applicants disclosed and claimed invention:

> "A method for forming a copper damascene feature with improved electrical properties including reducing moisture and etching residues from a damascene opening"

On the other hand, Rozbiki et al. discloses a process for depositing a copper seed layer by PVD while passivating the copper seed layer during or immediately after the deposition to prevent excessive oxidation (see Abstract). Rozbiki et al. also disclose a cleaning process carried out on copper exposed underlying the damascene opening to remove copper oxides by a physical sputter etch **and/or** a hydrogen based plasma treatment (col 5, lines 40-49). Thus, Rozbiki et al. seem to imply exposure of the underlying exposed copper to an oxidizing

atmosphere **prior to cleaning**. Rozbiki et al. also disclose that "the precleaning process typically involves degassing".

Rozbiki et al. fails to disclose several aspects of Applicants disclosed and claimed invention including:

"etching through an etch stop layer at the at least one damascene opening bottom portion to expose an underlying copper area;

then carrying out a sub-atmospheric DEGAS process in-situ with simultaneous heating of the process wafer in a hydrogen containing ambient;

then carrying out an in-situ sputter-clean process; and,

then forming a barrier layer in-situ to line the ~~dual~~ damascene opening."

There is no apparent motivation or suggestion for combining Kim et al. and Rozbiki et al. other than Applicants disclosed and

claimed invention. For example, there is no apparent motivation for combining the teachings of Kim et al. who teach a **degas process under high vacuum** followed by a sputter clean process using a plasma including hydrogen, where both steps are performed on a copper seed layer **following deposition** of a **copper seed layer on a barrier layer** and the teachings of Rozbiki et al. who teach a pre-cleaning process **prior to copper seed layer deposition** using a hydrogen based plasma and who generally disclose a degas process as part of the cleaning process.

The attempted combination of the teachings of Kim and Rozbiki et al. would change the principal of operation of both Kim and Rozbiki et al. making both unsuitable for its intended purpose.

Even Assuming *arguendo* proper motivation for combining the teachings of Kim and Rozbiki et al., such combination fails to produce Applicants disclosed and claimed invention.

The combination of Kim and Rozbiki et al. nowhere teaches or suggests carrying out a **sub atmospheric** DEGAS process with **simultaneous heating** in a **hydrogen containing ambient**.

Contrary to Examiners assertion, Rozbiki et al. do not teach heating the wafer in hydrogen ambient at (col 5, lines 40-49, and col 8, lines 59-60).

At col 8, lines 59-60, Rozbiki et al. discloses the conducting of experiments to demonstrate the passivation of copper seed layers, where **an unprocessed silicon dioxide semiconductor wafer** is degassed at 350 °C prior to depositing a barrier layer **in a different chamber**.

The combination of Kim and Rozbiki et al. nowhere teaches or suggests carrying out the above step **in-situ following etching** of the damascene opening.

The combination of Kim and Rozbiki et al. nowhere teaches or suggests forming the **barrier layer in-situ following the sputter clean process**.

Neither Kim nor Rozbiki et al., alone or inc combination, recognize the problem that Applicants have recognized and solved by their disclosed and claimed invention:

"A method for forming a copper damascene feature with improved electrical properties including reducing moisture and etching residues from a damascene opening"

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

"The fact that references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." *Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).*

2. Claims 3-5, and 14-16, stand rejected under 35 USC Section 103(a) as being unpatentable over Kim (788) in view of Rozbicki et al. (US 6,554,914), as applied above to claim 1, and further in view of Kim (US 2004/0127002).

Applicants reiterate the comments made above with respect to Kim (788) and Rozbicki et al.

Kim (004) discloses an in-situ process whereby the process wafer is **cooled** following an etching process prior to an in-situ cleaning process using a **hydrogen containing plasma** at 25 to 50°C to remove polymer formed on sidewalls and metal oxide formed on a bottom portion. Kim (004) **teach a separate step of annealing the substrate** following the hydrogen plasma treatment (see Abstract;

paragraphs 0010, 0011, 0027). Kim (004) does not disclose carrying out the annealing treatment in hydrogen or at a sub-atmospheric pressure.

Even assuming *arguendo* a motivation for combining Kim (004) with either one of or both of Kim (788) and Rozbicki et al., such combination does not produce Applicants disclosed and claimed invention.

Moreover, Kim (004) teach directly away from Applicants disclosed and claimed invention by teaching a hydrogen plasma treatment at a **reduced temperature prior to** an **annealing process** where the atmosphere and pressure are not disclosed.

"A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention." *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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